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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/881,292	06/13/2001	John P. Blanks	1051-006/MMM	6769

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EXAMINER	
THOMSON, WILLIAM D	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 07/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/881,292	BLANKS, JOHN P.	
	Examiner	Art Unit	
	William D. Thomson	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 June 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/13/01*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-21 have been presented, examined and rejected.

Priority

2. Applicant's claim for domestic priority under 35 U.S.C. 119(e) is acknowledged. However, the provisional application upon which priority is claimed fails to provide adequate support under 35 U.S.C. 112 for claims 5, 7, 12, 14, and 19 of this application. Though the generic constructs are provided the specific mathematical analysis and equations resulting from that analysis are not expressly taught in the provisional application. It is also noted that Applicant did not incorporate the provisional application.

Information Disclosure Statement

3. The information disclosure statement (IDS), filed June 13, 2001, has been considered by the examiner.

Drawings

4. Figures 1-8, 10, 12, 14 and 15 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. This is primarily based upon applicant's own admissions to what is well known in the prior art. See M.P.E.P § 608.02(g). Corrected drawings in compliance with 37 C.F.R. 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 C.F.R. 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not

accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

5. Claim 1 is objected to because of the following informalities: the phrase "and the adjoint to it" is ambiguous. Examiner suggests changing the langue to positively recite what "it" is relative to adjoint model of the circuit. Depend claims 2-7 inherit this defect. Appropriate correction is required.

Claim Rejections - 35 U.S.C. § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

6. Claims 8-14 are rejected under 35 U.S.C. § 101 because they constitute purely mathematical algorithms that are disembodied from the technological arts and can be implemented as a series of mental and/or paper and pencil operations not performed on or with a machine . Moreover, these claims are abstractions of modeling sets of equations for designing circuits. See MPEP 2106 and specifically, for such subject matter to be statutory, the claimed process must be limited to a practical application of the abstract idea or mathematical algorithm in the technological arts. See Alappat, 33 F.3d at 1543, 31 USPQ2d at 1556-57 (quoting Diamond v. Diehr, 450 U.S. at 192, 209 USPQ at 10). See also Alappat 33 F.3d at 1569, 31 USPQ2d at 1578-79 (Newman, J.,

concurring) ("unpatentability of the principle does not defeat patentability of its practical applications") (citing O 'Reilly v. Morse, 56 U.S. (15 How.) at 114-19). A claim is limited to a practical application when the method, as claimed, produces a concrete, tangible and useful result; i.e., the method recites a step or act of producing something that is concrete, tangible and useful. See AT &T, 172 F.3d at 1358, 50 USPQ2d at 1452. Likewise, a machine claim is statutory when the machine, as claimed, produces a concrete, tangible and useful result (as in State Street, 149 F.3d at 1373, 47 USPQ2d at 1601) and/or when a specific machine is being claimed (as in Alappat, 33 F.3d at 1544, 31 USPQ2d at 1557 (in banc). For example, a computer process that simply calculates a mathematical algorithm that models noise is nonstatutory. However, a claimed process for digitally filtering noise employing the mathematical algorithm is statutory.

7. Claims 15 and 16-21 are rejected under 35 U.S.C. § 101 because they constitute a computer readable medium with software stored thereon, this constitutes sata structures not claimed as embodied in computer-readable media are descriptive material per se and are not statutory because they are not capable of causing *functional change in the computer.* See, e.g., Warmerdam, 33 F.3d at 1361, 31 USPQ2d at 1760 (claim to a data structure per se held nonstatutory). In contrast, a claimed computer-readable medium encoded with a data structure defines structural and *functional interrelationships between the data structure and the computer software and hardware components which permit the data structure's functionality to be realized, and is thus statutory.* If a claim defines a useful machine or manufacture by identifying the physical

structure of the machine or manufacture in terms of its hardware or hardware and software combination, it defines a statutory product. See, e.g., Lowry, 32 F.3d at 1583, 32 USPQ2d at 1034-35; Warmerdam, 33 F.3d at 1361-62, 31 USPQ2d at 1760. Office personnel must treat each claim as a whole. The mere fact that a hardware element is recited in a claim does not necessarily limit the claim to a specific machine or manufacture. *Cf. In re Iwahashi, 888 F.2d 1370, 1374-75, 12 USPQ2d 1908, 1911-12 (Fed. Cir. 1989), cited with approval in Alappat, 33 F.3d at 1544 n.24, 31 USPQ2d at 1558 n.24.* The software when executed on a computer imparts the functionality to the claimed invention. Moreover, the claims recite pure mathematical algorithms and are also non-statutory based upon the same reasoning as claims 8-14, *id*.

Claim Rejections - 35 U.S.C. § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1-21 are rejected under 35 U.S.C. § 102(b) as being clearly anticipated by Nguyen et al. (1998 article) and Conn (1997 article), individually.

Taking claim 1, for example, Nguyen et al. (1998) and Conn (1997), individually teach, An electronic circuit sensitivity analysis method for analyzing sensitivity of an electronic circuit model as represented by electronic circuit model data, having conducting a first computer simulation of the electronic circuit model and receiving

results of the first simulation identifying a nonlinear circuit element in the electronic circuit model and representing a nonlinear effect of the nonlinear circuit element by applying a corresponding voltage source to the electronic circuit model; generating an adjoint of the electronic circuit model based upon the results of the first simulation, including mapping the corresponding voltage source into a current source in the adjoint; conducting a second simulation of the adjoint of the electronic circuit model and receiving results of the second simulation; and conducting a circuit sensitivity analysis of the electronic circuit model based upon the results of the simulations of the electronic circuit model and the adjoint to it at Nguyen et al. (1998): Introduction, ACES (Adaptively Controlled Explicit Simulation) with adjoint transient sensitivity calculations and PWL approach, especially figures 1 and 3, Sections entitled "Overview of Adjoint Sensitivity Computations in ACES", "Piecewise Linear Adjoint Circuit elements", "Adjoint Circuit Excitations", and "Adjoint Sensitivity Algorithms", Figures 1, 2, and 3, equations 4, 5, 6, 7, 8, 9, 10, 11-17 ;and Conn (1997): Instruction and Motivation, JiffyTune and SPECS and LANCELOT implemented for circuit optimization via adjoint lagrangians, especially figure 1, Sections "Demonstration by means of an example", "Theory", "Features of JiffyTune", "Implementation" and "Results", equations 3-8, figures 1 and 2.

As to claim 2, Nguyen et al. (1998) and Conn (1997), individually teach, plural nonlinear circuit elements are identified in the electronic circuit model and non-linear effects of the plural nonlinear circuit elements are represented by applying plural corresponding voltage sources to the electronic circuit model; and an adjoint of the electronic circuit model is generated based upon the results of the first simulation,

including mapping the plural corresponding voltage sources into current sources in the adjoint at Nguyen et al. (1998): Introduction, ACES (Adaptively Controlled Explicit Simulation) with adjoint transient sensitivity calculations and PWL approach, especially figures 1 and 3, Sections entitled "Overview of Adjoint Sensitivity Computations in ACES", "Piecewise Linear Adjoint Circuit elements", "Adjoint Circuit Excitations", and "Adjoint Sensitivity Algorithms", Figures 1, 2, and 3, equations 4, 5, 6, 7, 8, 9, 10, 11-17 ;and Conn (1997): Instruction and Motivation, JiffyTune and SPECS and LANCELOT implemented for circuit optimization via adjoint lagrangians, especially figure 1, Sections "Demonstration by means of an example", "Theory", "Features of JiffyTune", "Implementation" and "Results", equations 3-8, figures 1 and 2.

As to claim 3, Nguyen et al. (1998) and Conn (1997), individually teach, the current source in the adjoint to which the corresponding voltage source is mapped is a current-controlled current source at Nguyen et al. (1998): Introduction, ACES (Adaptively Controlled Explicit Simulation) with adjoint transient sensitivity calculations and PWL approach, especially figures 1 and 3, Sections entitled "Overview of Adjoint Sensitivity Computations in ACES", "Piecewise Linear Adjoint Circuit elements", "Adjoint Circuit Excitations", and "Adjoint Sensitivity Algorithms", Figures 1, 2, and 3, equations 4, 5, 6, 7, 8, 9, 10, 11-17 ;and Conn (1997): Instruction and Motivation, JiffyTune and SPECS and LANCELOT implemented for circuit optimization via adjoint lagrangians, especially figure 1, Sections "Demonstration by means of an example", "Theory", "Features of JiffyTune", "Implementation" and "Results", equations 3-8, figures 1 and 2.

As to claim 4, Nguyen et al. (1998) and Conn (1997), individually teach, the nonlinear effect of the nonlinear circuit element is characterized by a nonlinear admittance at Nguyen et al. (1998): Introduction, ACES (Adaptively Controlled Explicit Simulation) with adjoint transient sensitivity calculations and PWL approach, especially figures 1 and 3, Sections entitled "Overview of Adjoint Sensitivity Computations in ACES", "Piecewise Linear Adjoint Circuit elements", "Adjoint Circuit Excitations", and "Adjoint Sensitivity Algorithms", Figures 1, 2, and 3, equations 4, 5, 6, 7, 8, 9, 10, 11-17 ;and Conn (1997): Instruction and Motivation, JiffyTune and SPECS and LANCELOT implemented for circuit optimization via adjoint lagrangians, especially figure 1, Sections "Demonstration by means of an example", "Theory", "Features of JiffyTune", "Implementation" and "Results", equations 3-8, figures 1 and 2.

As to claim 5, Nguyen et al. (1998) and Conn (1997), individually teach, the equivalent relationships of this equation at Nguyen et al. (1998): Introduction, ACES (Adaptively Controlled Explicit Simulation) with adjoint transient sensitivity calculations and PWL approach, especially figures 1 and 3, Sections entitled "Overview of Adjoint Sensitivity Computations in ACES", "Piecewise Linear Adjoint Circuit elements", "Adjoint Circuit Excitations", and "Adjoint Sensitivity Algorithms", Figures 1, 2, and 3, equations 4, 5, 6, 7, 8, 9, 10, 11-17 ;and Conn (1997): Instruction and Motivation, JiffyTune and SPECS and LANCELOT implemented for circuit optimization via adjoint lagrangians, especially figure 1, Sections "Demonstration by means of an example", "Theory", "Features of JiffyTune", "Implementation" and "Results", equations 3-8, figures 1 and 2.

As to claim 6, Nguyen et al. (1998) and Conn (1997), individually teach, the nonlinear effect of the nonlinear circuit element is characterized by a nonlinear impedance at Nguyen et al. (1998): Introduction, ACES (Adaptively Controlled Explicit Simulation) with adjoint transient sensitivity calculations and PWL approach, especially figures 1 and 3, Sections entitled "Overview of Adjoint Sensitivity Computations in ACES", "Piecewise Linear Adjoint Circuit elements", "Adjoint Circuit Excitations", and "Adjoint Sensitivity Algorithms", Figures 1, 2, and 3, equations 4, 5, 6, 7, 8, 9, 10, 11-17 ;and Conn (1997): Instruction and Motivation, JiffyTune and SPECS and LANCELOT implemented for circuit optimization via adjoint lagrangians, especially figure 1, Sections "Demonstration by means of an example", "Theory", "Features of JiffyTune", "Implementation" and "Results", equations 3-8, figures 1 and 2.

As to claim 7, Nguyen et al. (1998) and Conn (1997), individually teach, equivalent relationships of this equation at Nguyen et al. (1998): Introduction, ACES (Adaptively Controlled Explicit Simulation) with adjoint transient sensitivity calculations and PWL approach, especially figures 1 and 3, Sections entitled "Overview of Adjoint Sensitivity Computations in ACES", "Piecewise Linear Adjoint Circuit elements", "Adjoint Circuit Excitations", and "Adjoint Sensitivity Algorithms", Figures 1, 2, and 3, equations 4, 5, 6, 7, 8, 9, 10, 11-17 ;and Conn (1997): Instruction and Motivation, JiffyTune and SPECS and LANCELOT implemented for circuit optimization via adjoint lagrangians, especially figure 1, Sections "Demonstration by means of an example", "Theory", "Features of JiffyTune", "Implementation" and "Results", equations 3-8, figures 1 and 2.

Claims 8-21 are rejected based upon the same reasoning as claims 1-7. Claims 8-21 recite the same limitations as claims 1-7 and therefore are rejected based upon the same teachings in Nguyen et al. (1998) and Conn (1997), individually, at Nguyen et al. (1998): Introduction, ACES (Adaptively Controlled Explicit Simulation) with adjoint transient sensitivity calculations and PWL approach, especially figures 1 and 3, Sections entitled "Overview of Adjoint Sensitivity Computations in ACES", "Piecewise Linear Adjoint Circuit elements", "Adjoint Circuit Excitations", and "Adjoint Sensitivity Algorithms", Figures 1, 2, and 3, equations 4, 5, 6, 7, 8, 9, 10, 11-17 ;and Conn (1997): Instruction and Motivation, JiffyTune and SPECS and LANCELOT implemented for circuit optimization via adjoint lagrangians, especially figure 1, Sections "Demonstration by means of an example", "Theory", "Features of JiffyTune", "Implementation" and "Results", equations 3-8, figures 1 and 2.

Conclusion

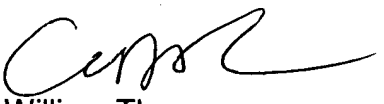
9. The prior art made of record, on the accompanying PTO 892, and not relied upon is considered pertinent to applicant's disclosure.

CONTACT INFORMATION

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to William D. Thomson whose telephone number is 571-272-3718. The examiner can normally be reached on 8:30-3:30 Moday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo Picard can be reached on 571-272-3749. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



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